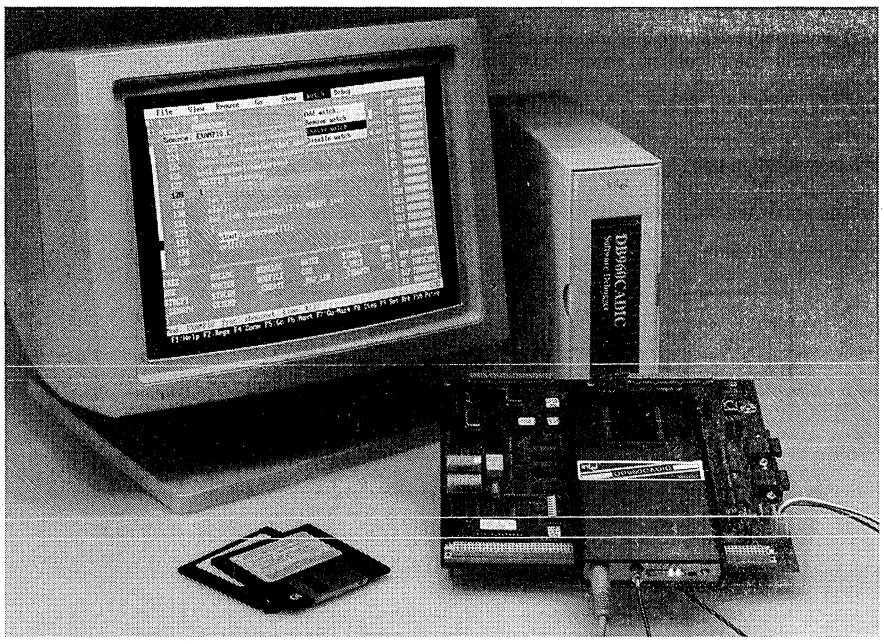
DB960CADIC IN-CIRCUIT DEBUG MONITOR



280900-1

DB960CADIC

Intel's DB960CADIC, the in-circuit debug monitor for the 33 MHz i960CA embedded microprocessor, represents a new generation of development tool technology.

DB960CADIC allows users to debug high-speed, cached applications at the full speed of the i960CA target processor. Controlled by Intel's DB interface, DB960CADIC offers the user a tool with a powerful feature set at a fraction of the cost of traditional development tools. DB960CADIC is designed to improve productivity by allowing the user to debug software before and after the target system arrives, with minimal hardware intrusion.

Features

- Real-time emulation of the i960CA embedded microprocessor at speeds up to 33 MHz
- Full development and debug support for i960CA on-chip cache and RAM
- Minimal intrusive operation, allowing the user to debug the target system with minimal modification subject to initial design constraints
- Breakpoint capabilities include ten software breakpoints, two hardware execution address breakpoints, and two hardware data address breakpoints. The human interface supplements these breakpoints with the ability to break on data values, conditions, and a four-state state machine in non-real time.
- Low-Cost
- Source-Level, Symbolic Debugging in a Windowed Human Interface with pull down Menus (DB). This interface is consistent across i960CA tools.
- 128K Bytes User Memory
- Virtual I/O, the ability to perform I/O between the DB960CADIC unit and the host
- In-Circuit operation facilitates easy transition between target systems
- Optional Stand-Alone Self-Test (DB960CASAST) Module
- Optional Logic Analyzer Interface Board (LAI960CA)

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DB960CADIC IN-CIRCUIT DEBUG MONITOR

Full-Speed Debug and Development

The DB960CADIC In-Circuit Debug Monitor provides sophisticated real-time hardware and software debug capabilities for i960CA embedded microprocessor-based designs. The user can run at the full speed of the target processor, ensuring that elusive timing bugs will be found. The DB960CADIC is jumpered to receive a clock pulse from either the user's target system, or from an internal 25 MHz clock.

Ideal for All Stages of Development

DB960CADIC can be used by both hardware and software developers, at any stage of design. Early in the development process, DB960CADIC allows software debugging when inserted into an existing i960CA board such as the DB960CASAST module or the EV80960CA board. Later in the design cycle, DB960CADIC can be inserted into the user's target system, thus facilitating debug of hardware/software integration.

Speed Development with Source Code, Symbolic Debugging

Using source code oriented debugging in a windowed, symbolic interface, software engineers can increase productivity by debugging in the medium they are familiar with, software source.

Commands can be entered via either function keys, pull-down menus which group logically related commands, or a supplementary command line which allows entry of complex conditions. In addition, source code symbolics can be used to examine and modify memory and registers. Optimal symbolic debugging can be achieved when using DB960CADIC with genuine Intel languages.

Powerful Break Capabilities

DB960CADIC provides complex emulation control by utilizing the on-chip debug registers within the i960CA. Real-time break capabilities include the ability to break on any two execution addresses or data access addresses in hardware. Software breakpoints are also used to supplement the hardware breakpoints for RAM-based memory subsystems. DB960CADIC extends these capabilities by providing the ability to break on data values, NOT data values, or combinations of the above in a four-state state machine. More complex conditions such as breaking when a variable is less than a certain value can be entered via a very flexible feature called conditional breakpoints.

128K Bytes User Memory

DB960CADIC provides the user with 128K bytes of memory in Region F of the i960CA target space. Since the debug monitor is also placed in Region F, the on-chip bus interface unit of the i960CA is configured to address region F as byte-wide memory with 5 waitstates and no burst accesses allowed.

Virtual Input/Output

DB960CADIC is shipped with documented library calls which provide users with a built-in mechanism of performing target I/O using the host system. These libraries provide the ability to simulate I/O operations in the target system before target hardware is available.

High Speed Serial Link

Communication between a host and the DB960CADIC module is supported via RS232 and RS422 communication links. RS232 allows access to industry standard serial protocols while the RS422 link provides a higher speed communication mechanism currently emerging in the development market. PC/AT Compatible RS422 communication boards are available from various third party vendors.

Optional Stand-Alone Self Test Chassis

An optional stand-alone self test chassis complements DB960CADIC by allowing the user to debug and test code before prototype hardware is available. The DB960CASAST includes self-test circuitry to ensure that the DB960CADIC unit is working correctly. It also provides 4 Megabyte of DRAM to be used for

DB960CADIC IN-CIRCUIT DEBUG MONITOR

developing applications. This memory has a (3,1,1,1) waitstate pattern at 25 MHz. This waitstate pattern is programmable using the bus controller unit in the i960CA. It also includes an 8254 programmable timer which can optionally interrupt the i960CA processor and provide the ability to time code sequences.

Optional Logic Analyzer Interface Board

The LAI960CA board provides access to i960CA pins by routing the signals to easily accessible stake pins while passing them through to the target system.

Software Completes the System

Intel provides a comprehensive software development environment to complement DB960CADIC. This environment includes C and ASM source languages, a retargetable debug monitor, and DB960CADIC. The languages support the entire range of 80960 embedded processors.

Worldwide Service, Support, and Training

To augment its development tools, Intel offers a full array of seminars, classes, workshops, field application engineering expertise, hotline technical support, and on-site service.

Intel also offers a Software Support contract which includes technical software information, telephone support, automatic distributions of software and documentation updates, *iCOMMENTS* publication, remote diagnostic software, and a development tools troubleshooting guide.

Intel's 90-day Hardware Support package includes technical hardware information, telephone support, warranty on parts, labor, material, and on-site hardware support.

Intel Development Tools also offers a 30-day, money-back guarantee to customers who are not satisfied after purchasing any Intel development tool.

DB960CADIC SPECIFICATIONS AND REQUIREMENTS

Host System Requirements

Host system requirements to run the in-circuit debugger include the following:

—DOS version 3.2 or later excluding DOS 4.0

—640 bytes of RAM in conventional memory

—A 20 MB hard disk

—An RS232 or RS422 Serial Port

Evaluated Systems include:

Intel 301/302* with DOS 3.3

IBM Personal System/2* Model 70/80 with DOS 4.01

Environment Characteristics

Operating Temperature:	+10°C to +40°C (50°F to 104°F)
Operating Humidity:	Maximum of 90% relative humidity, non-condensing.

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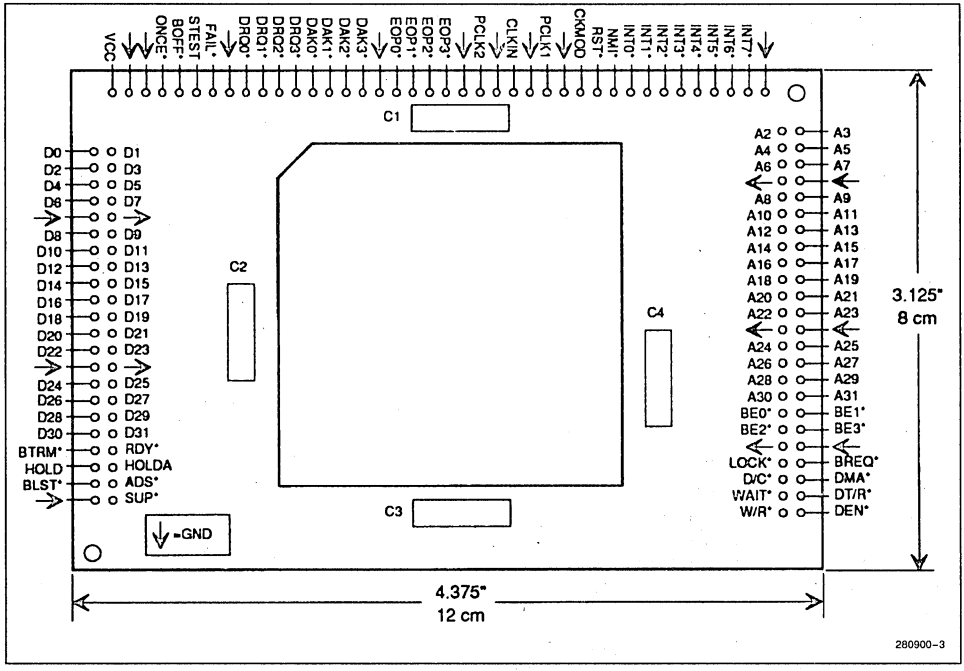

Figure 1

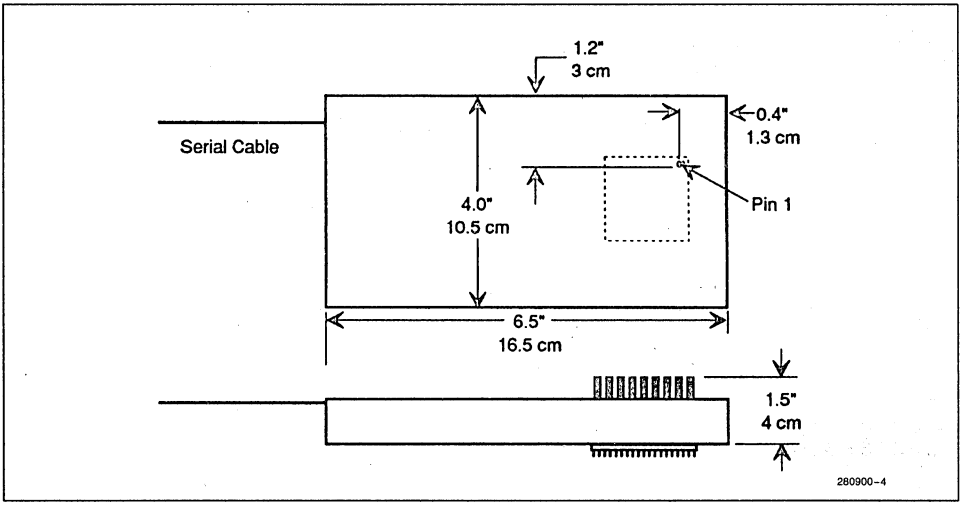

Figure 2

DB960CADIC IN-CIRCUIT DEBUG MONITOR

DB960CADIC Interface Considerations

Target systems intended to receive DB960CADIC must meet the following requirements:

- The target system must not respond to memory accesses in Region F (0F0000000-0FFFFFFFF) with DB960CADIC installed. DB960CADIC provides an ACTIVE out signal which can be used to qualify bus logic to prevent this occurrence when DB960CADIC is installed.
- The Target System must provide 1.3 Amps of power (worst case) .9 Amps average to power the DB960CADIC unit.
- Use of one of the nine directly accessible i960CA interrupts.
- Use of interrupt table entry 242 or 248.
- Additional Signal Loading as follows:

The DB960CADIC makes use of the PCLK outputs, D0 through D7, and some of the address and control signals of the processor. The following table lists the worst case loadings added by the presence of the DB960CADIC circuitry.

Signal Name	DC Load (μA)	Capacitive Load (pF)
PCLK1	+25/−250	8
PCLK2	+30/−255	17
CLKIN	+12/−12	13
D0:D7	+20/−600	10
A31:26	+25/−250	11
A2:A17	+20/−100	10
BE0*, BE1*	+20/−100	10
ADS*	+50/−500	13
W/R*	+50/−500	13
WAIT*	+25/−250	8
BLAST*	+25/−250	8
FAIL*	+20/−20	8
RESET*	+15/−15	25
INT0:7*	+20/−500	15
NMI*	+20/−500	15

Additional Loading Imposed on the Target by the DB960CADIC

Ordering Information

DB960CADIC	In-circuit debug monitor for the i960CA embedded microprocessor. Operates at speeds up to 33 MHz. Includes hardware debug module, RS232/RS422 serial cables, DOS host software, and documentation.
DB960CASAST	Stand-Alone Self Test Unit for DB960CADIC. Includes built-in power supply, self-test board, 4Mbyte of usable DRAM for code development, and enclosure.
DB960CAST	DB960CADIC and DB960CASAST as described above.
LAI960CA	Optional Logic Analyzer Interface Board for the i960CA system. Does not require DB960CADIC.